REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 4 and 6 stand objected to as lacking sufficient antecedent basis and for an identified informality, respectively. Claims 1-3 and 5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,889,291 to Palanca et al. ("Palanca"). Claims 4 and 6-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Palanca in view of U.S. Patent No. 6,195,106 to Deering et al. ("Deering").

By this amendment and response, Applicants cancel claims 1-11 without prejudice. Accordingly, the aforementioned objections and rejections are moot.

As to newly submitted claim 12, Applicants respectfully submit that no combination of the cited prior art, alone and in combination, appears to teach or suggest the claimed memory architecture comprising "a level one cache comprising texel information; a level two cache ... that comprises overlapping fetched texel information resulting from execution of previous memory fetch instructions; and wherein when the level one cache does not comprise overlapping fetched texel information requested by a subsequent memory fetch instruction, the level two cache is operative to transmit the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one cache."

As best understood by Applicants, Deering is directed toward a graphics system with multiported pixel buffers for accelerated pixel processing. The graphics system employs at least one frame buffer dynamic random access memory (FBRAM) that implements two levels of internal pixel caches (*see* Abstract) wherein the highest pixel access speeds to FBRAM chips are obtained if addressed pixels are present in an L1 pixel cache. If the pixels are not present in the L1 pixel cache, Deering teaches that the addressed pixel is transferred from the L2 pixel cache to the logical L1 pixel cache and the missing block is written back to the L2 pixel cache. If the

logical L2 pixel cache does not contain the required block, then the required block is read from the DRAM. (Col. 10, ll. 40-53).

Palanca is directed toward a method and apparatus for cache replacement for a multiple variable-way associative cache where a cache array is partitioned based upon requests for memory from an integrated device having a plurality of processors. (*See* Abstract). The system includes an L1 cache and an L2 cache where the L2 cache is a multiprocessor L2 cache for sharing among at least a CPU and a graphics processor. (Col. 4, ll. 48-62).

Applicants respectfully submit that the cited prior art, alone and in combination, does not appear to teach or suggest a level one cache comprising texel information; a level two cache ... that comprises overlapping fetched texel information resulting from execution of previous memory fetch instructions. Accordingly, for at least these reasons, the cited prior art, alone and in combination, also fails to teach or suggest wherein when the level one cache does not comprise overlapping fetched texel information requested by a subsequent memory fetch instruction, the level two cache is operative to transmit the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one cache.

Accordingly, claim 12 is believed to be allowable over the cited prior art.

As to newly submitted claim 16, Applicants respectfully repeat the relevant remarks made above with respect to claim 12. Accordingly, Applicants respectfully submit claim 16 for allowance.

Claims 13-15 and 17-22 depend upon allowable claims 12 and 16 and further contain additional novel and nonobvious subject matter not disclosed or suggested by the cited prior art. For at least this reason and those cited above with respect to claims 12 and 16, claims 13-15 and 17-22 are further believed to be allowable.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited

to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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